REMARKS

Status of Claims

Claims 1-18 were pending in this application at the time of the outstanding Office Action. Claims 11-18 have been withdrawn from consideration. Claims 2 and 4 are cancelled. Thus, Claims 1, 3 and 5-10 remain for examination.

Drawings

Figure 18 has been labeled as "Prior Art" as requested by the Examiner.

Claim Objections

Applicant has amended Claims 1, 5, 7, 9 and 10, to overcome the objections noted in the Office Action. As amended, Claim 1 recites that the recited transistors are operated by a "common voltage generated by a power source." To clarify what differentiates the recited transistors from one another, Claim 1 is amended to recite that at least some of the recited transistors have a gate dielectric layer of different thickness. Under these amendments to Claim 1, Claims 7 and 9 are consistent with Claim 1; for example, two of the transistors recited in Claim 1 can have the same gate dielectric layer thickness. The above amendments also address objections noted in the Office Action regarding to Claim 2, which has been cancelled in this amendment.

Applicant respectfully submits that the PTO, in its objection to Claim 1, has misinterpreted Applicant's characterization of the recited transistor that serves as the power source protection element. The specification characterizes said transistor as, for example, an "N-channel transistor of a diode connection type." The depiction of said transistor in Fig. 2 is consistent with this characterization. Applicant submits that, contrary to the indication in the Office Action, the specification and the drawings do not characterize said transistor as a MOS diode.

Applicant acknowledges with appreciation the suggested modifications regarding Claims 5 and 10. Per this amendment, the term "I/O interface region" replaces the previous term "I/O port."

Rejections Under § 112

Applicant submits that the above amendments to Claim 1 pertaining to the thickness of the transistor gate dielectric layer overcome the rejection of Claim 1 under § 112. Therefore, Applicant respectfully requests that this § 112 rejection be withdrawn.

Rejections Under § 102(e)

The Office Action rejects Claim 1 under 35 U.S.C. § 102(e) as being unpatentable over Lin et al., U.S. Patent Application Publication No. 2003/0173630. Applicant has amended Claim 1 to overcome this rejection.

As amended, Claim 1 recites that "said one transistor selected as the power source protection element has a higher threshold voltage among any transistors having said minimum thickness gate dielectric layer." Applicant submits that the device disclosed in Lin does not comprise the noted feature and therefore respectfully requests that the rejection under § 102(e) be withdrawn.

Rejections Under § 103(a)

The Office Action rejects Claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Lin , in view of prior art such as Nojiri, U.S. Patent Application Publication No. 2001/0045670. The Office Action also rejects Claims 2-4 and 6-10 under § 103(a) based on Applicant's admitted prior art ("AAPA") in view of Lin and/or Cheng et al, U.S. Patent No. 6,465,308 B1. In light of the current amendment, Applicant respectfully requests that these rejections be withdrawn.

As to Claim 5, the Office Action alleges that it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate an I/O port area around the device disclosed in Lin. Applicant submits that, as explained earlier, Claim 1,

from which Claim 5 depends, is amended to better differentiate Applicant's independent Claim 1 over the prior art. As amended, Claim 1 recites that the "said one transistor selected as the power source protection element has a higher threshold voltage among any transistors having said minimum thickness gate dielectric layer." Thus, Applicant submits that the device disclosed in Lin does not comprise the above feature. Even accepting an opposing view for the sake of argument, Applicant submits that a person of ordinary skill in the art would not be motivated to combine the teaching of Lin and Nojiri in order to arrive at Applicant's claimed invention. Indeed, nothing within the references themselves would lead one or motivate one to combine the teachings in the manner presented by the Examiner. In re Sernaker, 217 U.S.P.Q. 1, 13 (Fed. Cir. 1983). Thus, it is respectfully submitted that the Patent and Trademark Office has not made out a *prima facie* case of obviousness under the provisions of § 103 and that the rejection of Claim 5 must be withdrawn.

As to Claim 2, the Office Action relies on Cheng as disclosing the means of optimizing the threshold voltage of a transistor based on its application voltage. (The limitations of Claim 2 have now been incorporated into amended Claim 1.) Even accepting this view for the sake of argument, however, the isolated and broad teaching of such optimization fails to teach, describe or suggest the feature of Applicant's invention, noted above, that is absent from Lin. Cheng simply fails to disclose selecting as the power source protection element one transistor having a "higher threshold voltage among any transistors having said minimum thickness gate dielectric layer." Accordingly, the cited combination fails to establish a *prima facie* case of obviousness.

Applicant has amended Claim 3 to remove the process limitation objected to by the Examiner.

Regarding Claim 8, the Office Action alleges that the leak current of the transistor selected as the power source protection element in the "collectively taught" invention would be "naturally smaller" than that of the high speed processing type transistor because the protection element transistor has a higher threshold voltage than that of the high speed processing type transistor. For reasons explained above, Applicant submits that the invention is not collectively taught by prior art disclosed by Applicant and the Patent and Trademark

Office. Claim 8 depends from Claim 1 and is deemed patentable for the same reasons applicable to Claim 1. Applicant therefore submits that it would not be obvious to one of ordinary skill in the art at the time the invention was made to select a transistor as the power source protection element based on the value its leak current relative to a high speed processing type transistor.

For the above reasons, Applicant respectfully submits that the Patent and Trademark Office has not made out a *prima facie* case of obviousness under the provisions of 35 U.S.C. § 103 and that the rejections of Claims 3 and 6-10 must be withdrawn.

Conclusion

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

If any extensions of time are needed for timely acceptance of papers submitted herewith, applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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